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RESEARCH ARTICLE

EFFICIENT TRANSFORMERLESS SUPER JUNCTION MOSFET INVERTER

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ABSTRACT

The uni-polar sinusoidal pulse width modulation full- bridge transformer-less photovoltaic (PV) inverter can achieve high efficiency by using latest super junction metal–oxide– semiconductor field-effect transistor (MOSFET) together with silicon carbide (SiC) diodes. Though, the MOSFETs are definite to use in transformer-less PV inverter due to the low reverse- recovery characteristics of the body diode. In this paper, family of new transformer-less PV inverter topology for a grid-tied operation is projected by the super-junction MOSFETs and diodes as there is no requirement of reverse-recovery response for the main power switches for unity power operation. The added clamping branch clamps the freewheeling voltage at the half of dc input volt age during the freewheeling period. As a conclusion, the common-mode voltage kept constant during the whole grid period that reduces the leakage current considerably. Furthermore, dead time is not important for main power switches at both the high-frequency commutation and the grid zero crossing instant, results low-current deformity at output. Finally, a 1-kW prototype is built and tested to verify the theoretical analysis. The experimental results show 98.5% maxi mum efficiency and 98.32% European efficiency. In addition, to show the effectiveness, the proposed topology is compared with the other transformer-less topologies.

INTRODUCTION

RECENTLY, transformer-less inverter has been found as one of the excellent solutions for grid-tied photovoltaic (PV) application because of its higher conversion efficiency, lower cost, smaller size, and light weight if compare with one's consist transformer (Islam *et al*., 2015; Patrao *et al*., 2011). However, the main drawback of transformer-less inverter is the leakage current issues that need to be addressed very carefully. Due to the galvanic isolation losses between the PV module and the grid, a direct path is formed to flow leakage current which commonly depends on the non-negligible parasitic capacitance between the PV module, the ground, and the amplitude of fluctuating common-mode (CM) voltage. The fluctuation of common mode voltage confide on the topology structure and the control scheme. The leakage current flowing through the system increases grid current harmonics and system losses. where strong conducted and radiated electromagnetic interference are created, and more significantly, gives rise to safety issues (Li *et al*., 2013; Islam *et al*., 2015). Another important concern of transformer-less inverter is the efficiency that can be improved by the optimal design. Most of the inverters described in the literature and commercially available show the European efficiency in the range of 96%−98% (Xiao *et al*., 2014; Huafeng, 2015). These two issues (efficiency and leakage current) are the major force in pushing progressive development of a transformer-less grid-tied PV inverter (Islam *et al*., 2015; Xiao *et al*., 2014; Huafeng *et al*., 2015).

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In order to reduce the leakage current, a lot of in-depth researches have been conducted in the literature (Huafeng *et al*., 2015; Baojian, 2013; Barater, 2014; Huafeng, 2011; Kerekes, 2011; Alajmi, 2013; Bin, 2013; Bo, 2012; Chen *et al*., 2015; Freddy *et al*., 2014), where a new freewheeling path has been introduced to decouple PV module from the grid during the freewheeling period. However, the switches junction capacitance that cannot be ignored in the practical application may have an impact on the leakage current (Bo, 2012), It is presented in that to completely eliminate the leakage current, the CM voltage needs to be clamped to the midpoint of the dc input voltage instead of only disconnecting the PV module from the grid. On the other side, to improve the efficiency, the transformer- less inverter can be implemented using super-junction MOSFET and SiC diodes. The super-junction MOSFETs is used to avoid fixed voltage drop and turn-off losses caused by tail current, thereby reducing conduction and switching losses. However, due to poor reverse recovery of MOSFETs slow body diode, is limited to use in transformer-less type of inverter. In this, Transistor based topologies grid-tied PV application is inspected and discussed based on their circuit structure, efficiency, and the voltage clamping capability. The most attractive type transformer-less topology is highly efficient and presumable. The inverter concept (HERIC) topology. This topology has been implemented in some commercial inverters, especially those from Sunway's converter. Two switches are added in the ac side of a full-bridge (FB) topology to decouple the PV module from the grid during the freewheeling period. Though the PV module is decoupled from the grid, a fluctuating CM voltage could be observed be- cause the freewheeling path potential is not

clamped at the half of dc input voltage. As seen in Fig. 1(b), the topology which has been proposed in (10) replaces the two switches freewheeling branch with one bidirectional switch and four diodes called H- bridge zero-voltage rectifier (HB-ZVR) topology. Also, another diode (D5) has been added for better eliminating the leakage current. The clamping function of this topology has been done using D5 which allows one-directional clamping, only if the freewheeling path potential (VAN ≈ VBN) is higher than the dc-link midpoint voltage. As a result, CM voltage fluctuation could be observed when the reverse condition is occurred which is very less than HERIC topology. In these two topologies, the grid current flows through two switches during the whole grid period; as a result, conduction loss is low.

MODE 1 OPERATION TO MODE 5 OPERATION

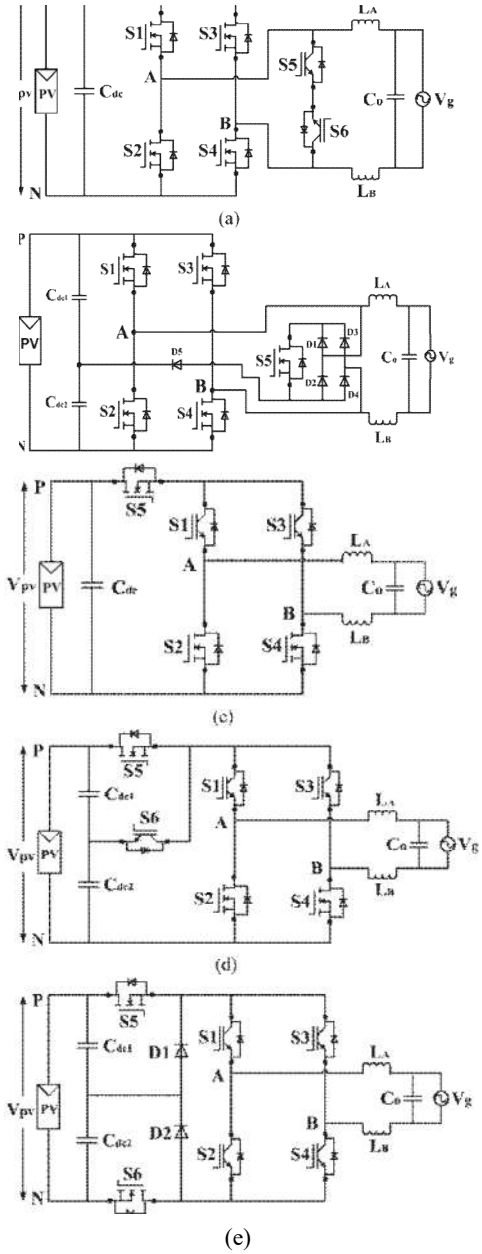


Fig.1. Different Modes of Operation

Fig. 1(c) shows another explicit transformer-less topology proposed in called H5 topology, made up by adding an extra switch in the dc side of an FB inverter.

In this topology, the freewheeling current flows through S1 and body diode of S3 during positive half cycle, and S3 and body diode of S1 during negative half cycle. As a result, the switches S1 and S3 could not be implemented with MOSFETs due to the low reverse re- covery of the MOSFET body diode. Another disadvantage is that the output current flows through three switches in the ac- tive mode for the complete grid cycle, thus higher conduction losses are present. A fluctuating CM voltage could also be ob- served because the freewheeling path potential is not clamped at the midpoint of dc link. An extension of H5 topology is pre- sented in (9) called optimized H5 (oH5) topology, where an extra switch (S6) has been added with the H5 topology to clamp the CM voltage at the half of input voltage as demonstrated in Fig. 1(d). Unfortunately, a dead time must have to be added between the gate signals of the switches S5 and S6 to avoid the short-circuit of the input split capacitor Cdc1.

As a result, CM voltage fluctuates in dead time (Huafeng *et al*., 2011). Another disadvantage of this topology is that higher conduction losses still remain due to the grid current flows through three switches in the active mode. Gonzalez *et al*. proposed another topology in called full-bridge with dc bypass which is also named as H6 topology. It employs two switches and two diodes in the dc side of FB inverter. The CM characteristics of this topology are better than other topologies because of the bidirectional clamping branch. During this freewheeling mode, either diode D1 or D2 is conducted based on the freewheeling path potential (VAN ≈ VBN) is higher or lower than half of the dc-link voltage. In this topology, leakage current removal effect depends only on the turn-on speed of the clamping diodes. However, this topology can be implemented with two MOSFET switches (S5 and S6) only. In addition, the grid current flows through four switches, thus higher conduction losses are also present.

Considering the advantages and the drawbacks of the transformer-less inverter mentioned earlier, a family of new transformer-less topologies for a single-phase grid-tied PV system is proposed based on two asymmetric phase legs in this paper. The key features of the proposed inverter are: 1) no dead time is required because the switches in the same phase leg are never all turned-on during the same SPWM cycle; as a result, current distortion at output is lower, 2) the CM voltage is kept constant at half of the dc input voltage because of the added clamping branch, and 3) during the positive and negative half cycle, the inductor current flows through two and three switches, respectively, thus the conduction loss is lower. The detailed operation principles and the control scheme to reduce the dc current injection are described in this paper. An investigation has been conducted to calculate the device power losses and to make a detail comparison with the topologies presented in Fig. 1. Finally, the experimental results validate the proposed topology. At last, a comparison table has been summarized based on the experimental data to show the effectiveness of the proposed topology.This paper is structured as follows. The family of the new topology structure, operating principle, and the control scheme is presented in Section II. The leakage current for the proposed topology, and the power device loss calculation and comparison are investigated in Section III. The experimental results are given in Section IV and Section V concludes the paper.The main drawback is the need of high input voltages, which requires either a previous boost dc–dc stage or a large PV string.

On the other hand, the full-bridge topology requires half of the input voltage demanded by the half-bridge topology. The total

cost of the inverter. Another method employed to eliminate CM current is to directly connect PV negative terminal and the grid neutral point (Bo, 2012; Chen, 2015). In these topologies, the negative output voltage is generated by the virtual dc bus, where the energy is transferred from the real bus to the virtual one. These topologies can generate three- level output voltage when modulated with uni-polar SPWM. To further reduce the filter size and to achieve high-power transfer capabilities, multilevel inverters can be employed. A selected few existing topologies employing dc/ac decoupling, clamping, and ground connection are shown in Fig. 2. This paper proposes a novel multilevel transformer-less half-bridge topology, which employs ground connection between PV negative terminal and grid neutral point, thereby completely eliminating CM leakage current. Although being a half- bridge-based topology, the proposed inverter is devoid from the need of high input voltages. In this way, the advantages of the full-bridge and half-bridge-based solutions are combined together.

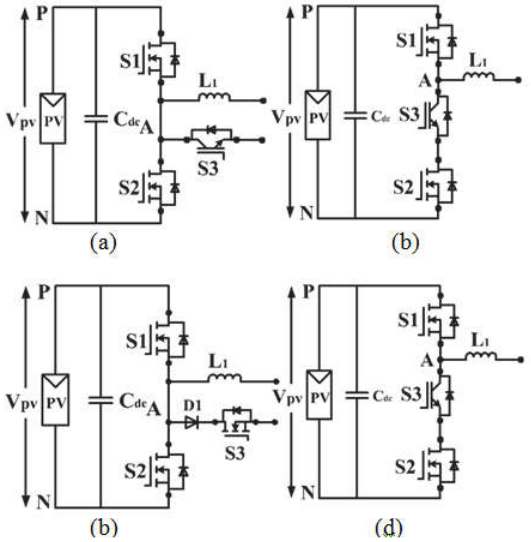


Fig. 2. Full Bridge And Half Bridge Topologies

Existing System

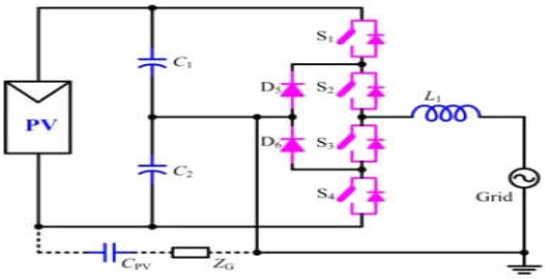


Fig. 3. Block Diagram of Existing System

However, the full bridge has to be modulated with bipolar sine pulse width modulation (SPWM) to avoid a varying CM voltage. As compared to the bipolar SPWM, the uni-polar SPWM exhibits superior performance in terms of the output current ripple, switching losses, smaller filter size, and no internal reactive power. Despite of such advantages, it cannot be directly employed in full-bridge transformer-less PV inverters since the CM voltage oscillates at switching frequency, which ultimately leads to high ground leakage currents. To block the CM current path during the freewheeling period, extra switches are inserted into the full-bridge inverter either on the dc or ac side.

Therefore, these full-bridge inverters can be further classified as dc decoupling based inverters and ac de- coupling based inverters, as described in (Kerekesm, 2011). However, in these topologies decoupling is incomplete due to the variable junction capacitance of the power switches leading to the flow of CM currents (6). To further reduce CM currents, some topologies clamp the CM voltage to half of the dc-link voltage during free- wheeling period (Alajmi, 2013; Bin, 2013). Although the active clamping based topologies can effectively reduce CM currents, they need two dc-link capacitors and some extra switches for clamping purpose, thereby increasing

Proposed System

The family of the proposed transformer-less PV inverter topology is depicted in Fig. 3 which is derived according to the derivation method described in the prior section, where S1 , S2 , S4 , and S5 are high-frequency switches, and S3 and S6 are low- frequency freewheeling switches. The unidirectional clamping branch is constructed using switch S7 and diode D3 with a capacitor divider (Cdc1 and Cdc2) which clamps the CM voltage at the midpoint of dc link. LA , LB , and Co make up the LC- type filter connected to the grid and Vpv

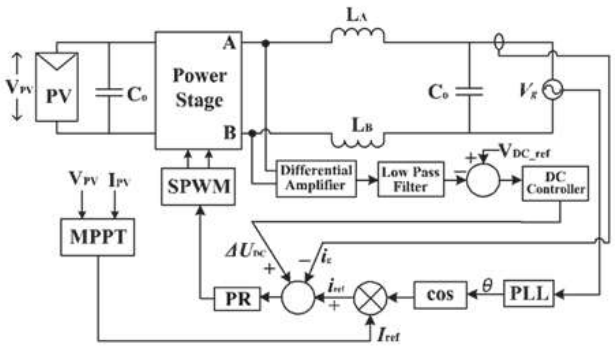


Fig. 4. Block Diagram of Proposed System

Control block of proposed Topology

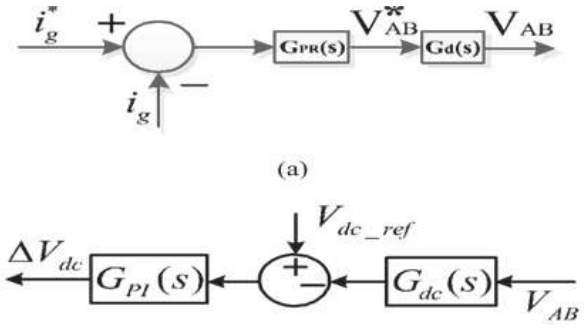


Fig. 5. Block diagram of the PR controller. (b) Block diagram of the dc suppression loop

In case of transformer-less inverter, dc current injection into the utility grid is an important issue that may cause saturation of distribution transformer, increased loss, and abnormal operation of the load connected to the grid. In order to suppress the dc cur- rent injection into the utility grid, several control strategies have been investigated in the literature. Based on the control technique proposed in, an improved control strategy, as depicted in Fig. 6, is implemented to control the proposed topology. The control block consists of a dc suppression loop, a grid current controller, and a phase-locked loop to synchronize with the grid current.

The dc suppression loop is composed of a differential amplifier, a low-pass filter, and a dc controller. Since the

output of the low-pass filter of dc suppression loop is constant in steady state, so a proportional- integral (PI) controller is used to control the dc-offset voltage. On the other hand, grid current is sinusoidal and the proportional-resonant (PR) controller has better performance of tracking the reference signal if compared to the normal PI controller and repetitive controller. Therefore, if compared with the control scheme proposed in , a PR controller is selected to control the grid current of the proposed topology. The block diagram of the

Complete control diagram of the proposed topology in a Laplace domain.

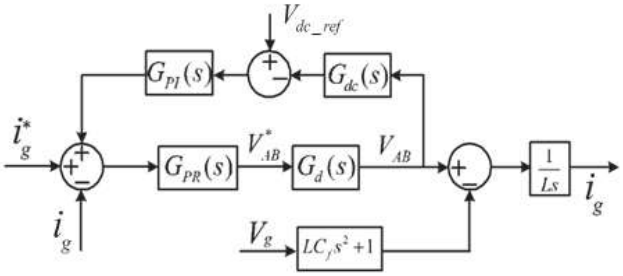


Fig. 6. Control Diagram of Proposed Topology

PR controller and dc suppression loop shown in figure, where GPR (s), Gd (s), and GPI(s) are the transfer function of fundamental current controller, processing and PWM delay, and offset voltage controller, respectively.

Leakage Current Analysis for the Proposed Topology

The PV module generates an electrically chargeable surface area which faces a grounded frame. In case of such configuration, a capacitance is formed between the PV module and the ground. Since this capacitance occurs as an undesirable side effect, it is referred as parasitic capacitance. Due to the loss of galvanic separation between the PV module and the grid, a CM resonant circuit can be created. An alternating CM voltage that depends on the topology structure and control scheme is used to electrify the resonant circuit and may lead to high ground Leakage.

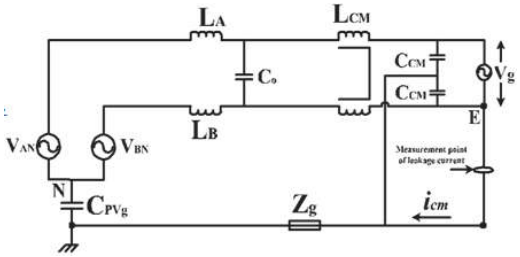


Fig. 7. Equivalent CM model of the proposed topology

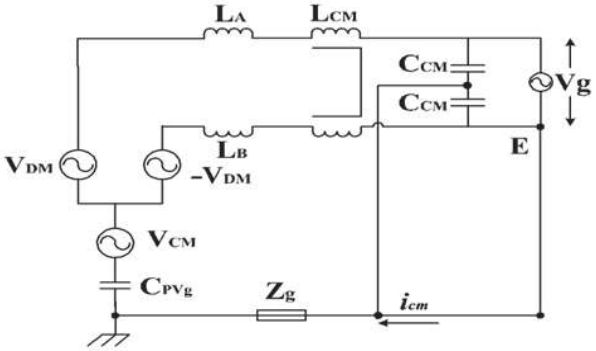


Fig. 8. Simplified single-loop CM model

Current. In order to analyze the CM characteristics, an equivalent circuit of the proposed topology as shown in Fig. 10 can be drawn, where VAN , and VBN are the controlled voltage source connected to the negative terminal N, LCM and CCM are the CM inductor and capacitor, CPVg is the parasitic capacitance, and Zg is the grid impedance.

Specification of the Prototypegpr

Inverter Parameter	Value
Input Voltage	400 VDC Grid
Voltage/Frequency	230 V/50 Hz Rated
Power	1000 W AC output
current	4.2 A Switching
Frequency	20 kHz DC bus capacitor
1 mF Filter capacitor	2.2 µF
Filter Inductor LA, LB	1 mH
PV parasitic capacitor Cpv1, Cpv2	75 nF
IGBT switches	STGW20NC60VD
MOSFET switches	SPW47N60C3
Diode (D1 –D2)	IDH08SG60C
Controller	dSPACE 1104

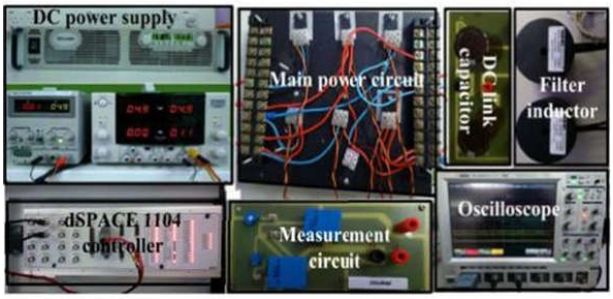


Fig. 9. Laboratory prototype

Power Devices Loss Calculation and Comparison

In this section, the device power losses for the H5, HERIC, H6, oH5, and proposed topologies are calculated for 5-kW rated power with the same circuit parameters given in Table III. It is necessary to take into account that the calculation of the losses is based on theory and its accuracy depends on the device datasheet accuracy. In Table I, the device type and their voltage stress, and distribution of the device number for different types of losses are given. It can be seen that the devices for switching loss for all the topologies are same but the other losses are different. The lowest conduction loss would be observed for HERIC topology as grid current flows only two switches, while the proposed topology takes place second position. However, it is noticeable that the zero-vector conduction loss of MOSFET + SiC diode freewheeling path for the proposed topology is less than the IGBT + body- diode freewheeling path of the HERIC, H5, H6, and oH5 topologies.

In order to calculate the power device losses, the IG- BTs are evaluated by STGW20NC60VD from STMICRO-ELECTRONICS with very soft ultrafast recovery anti-parallel diode. MOSFETs and diodes have been selected from Infineon with the model no SPW47N60C3 (70-mΩ on-resistance) and IDH08SG60C with no reverse recovery, respectively. The total power device losses at different output power for the H5, HERIC, H6, oH5, and proposed topologies are calculated under the same condition by extracting the parameters from the datasheet of the selected devices, which are given in Table II and shown as a histogram in Fig. 10. The calculation process and the theories are studied in details in the literature but not the contribution of this paper.

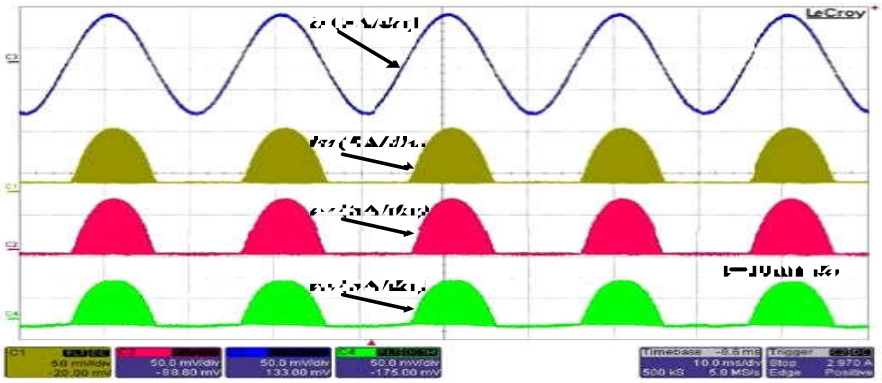
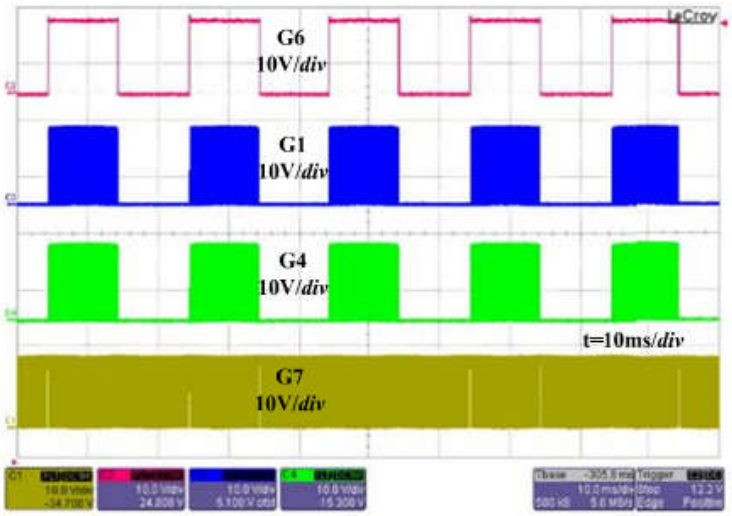
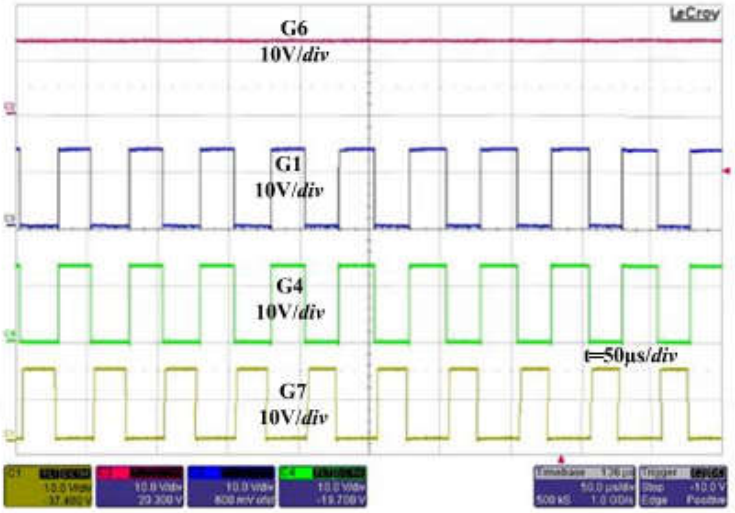
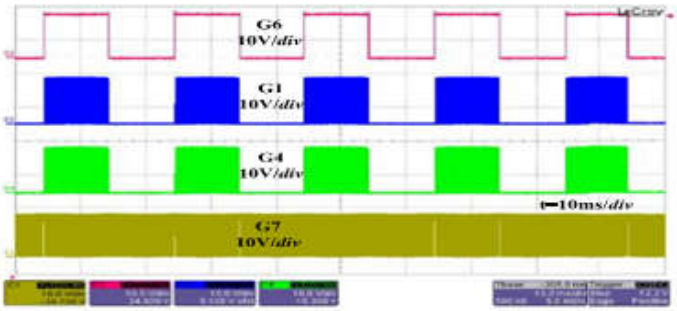


Fig.10. Wave Forms of The Different Inverters



(a)





(a)

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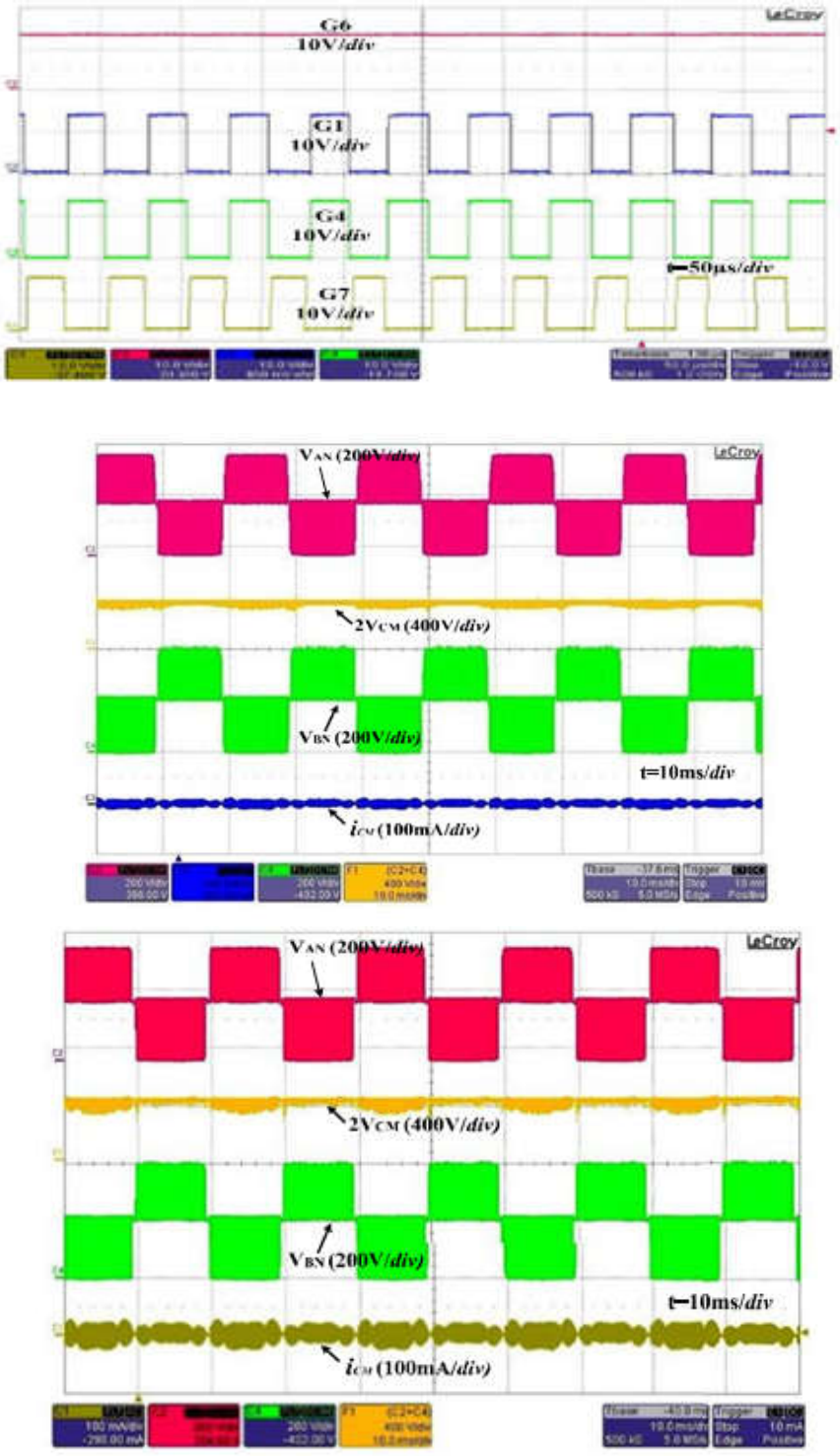

Fig. 11. Simulation results of inverters

Since all of the topologies have been implemented with the uni-polar SPWM technique with three-level output region is from 0.75μm to 1000 μm. voltage as +VPV, 0, and −VPV, and also identical filter inductor and capacitor values have been used; therefore, the losses across the output filter will be same for all the topologies which is neglected in this loss comparison. It can be seen that HERIC topology is with the least device loss, and the H5 and H6 topologies have the highest device loss as expected, while the proposed topology are in the second position. The precision power analyzer is used to measure the efficiency of the proposed inverter.

Note that the presented efficiency diagram covers the total power device losses and the filter inductor losses but it does not contain the losses for the control circuit. It is obvious that the efficiency of Experimental waveforms of VAN, VBN, VCM, and iCM for the pro- posed topology.

Experimental Results

In order to verify the performance of the proposed topology and to compare with other topologies, a universal prototype is built and tested. The photograph of the laboratory prototype is given in and the specifications are listed in Table III.

The capacitance between the PV module and the ground is emulated using a thin-film capacitor of 75 nF. The experimental gate signals of the proposed inverter are shown in. It is clear that the gate signals are in agreement with the theoretical analysis made in Section II and the gate drive voltages are kept at the desired level. while G7 is the contrary gate pulse of G1and G4 with a small dead band.

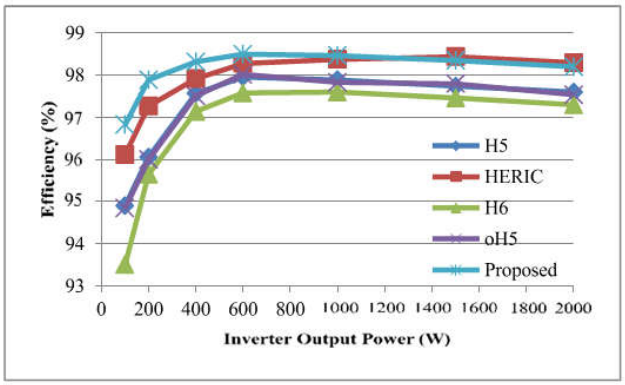

Fig. 12. Graph of different topologies

This shows that the switching voltages of the switches are half of the dc input voltage without any overstress. The partial expansion of is provided in showing that the switches S1 and S4 almost share the dc- link voltage when they commutate with oH5 topologies, The Experimental waveforms of VAN , VBN , VCM and iCM for the H6 topology. RMS value of leakage current is measured 15.5 and 18 mA, respectively. On the other hand, the RMS value of leakage current for the H5 and HERIC topologies reaches 45 and 48.8 mA, respectively. Therefore, it is clear that the leakage current flowing through the H5 and HERIC topologies is almost double compared to the proposed topology. In practical, additional CM filter is employed to the HERIC and H5 topologies to further suppress the leakage current.

The experimental waveform of the grid current ig and grid voltage vg are shown in case of full-load condition. It can be seen that vg and ig are in the same phase. The current harmonic distribution is depicted in, which shows that the total harmonic distribution is 1.7%. Therefore, it is clear that the proposed inverter can deliver PV power into the utility grid with low-harmonic distortion and unity power factor that can meet the requirement of IEEE Std 1547.1-2005, the inverter output voltage VAB has three levels, +VPV , 0, and −VPV . This designates that the proposed topology is modulated with uni-polar SPWM and the DM characteristics is excellent.

The efficiency of the H5, HERIC, oH5, H6, and proposed topologies are measured for power up to 2 kW and compared to verify the analysis made in Section III-B as illustrated in Experimental waveforms of VAN , VBN , VCM , and iCM for the pro- posed topology. The proposed topology at low power (<1200 W) is highest. This is due to low-freewheeling loss compared to the other topologies as described in Section III-B. However, at 2 kW, the efficiency of the HERIC topology is higher than the proposed topology which is due to the increased conduction loss. The maximum efficiency of the proposed topology is measured at 600 W and found to be 98.5%. It is clear that the lowest efficiency is measured with the H6 topology. On the other hand, H5 and oH5 topologies ensure almost same efficiency which is lower than HERIC and proposed topologies but exceeding H6 topology. The European efficiency is calculated by combining several weighted factors at various output power.

$$\eta EU = 0.03\eta 5\% + 0.06\eta 10\% + 0.13\eta 20\% + 0.10\eta 30\%$$

$$+0.48\eta 50\% + 0.2\eta 100\% .$$

The European efficiency for the H5, HERIC, H6, oH5, and proposed topologies is calculated 97.59%, 98.16%, 97.24%,97.55%, and 98.32%, respectively .

Conclusion

In this paper, a family of new efficient transformerless inverter for a grid-tied PV power generation system is presented using super junction MOSFETs as main power switches. The main advantages of the proposed topology is as follows: 1) High efficiency over a wide load range is achieved by using MOS-FETs and SiC diodes, 2) CM voltage remains constant during the operation modes due to the added clamping branch, which results low leakage current, 3) like as isolated FB inverter, excellent DM characteristics are achieved with uni-polar SPWM, and 4) PWM dead time is not required for main power switches, results low distortion at output. Finally, the proposed topology has been validated by a prototype rated 240/50 Hz 1 kW. The experimental results show 98.5% maximum efficiency and 98.32% European efficiency. Therefore, it can be concluded that the pro- posed inverter is very suitable for a single-phase grid-tied PV application.

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